AMENDMENTS TO THE SPECIFICATION

In the Specification

Please replace the second full paragraph of page 10 with the following amended paragraph:

Thus, each of the j-th divided signals SBj (where j: an integer of 2 to n) rises with being delayed the number of pulses $P_j=(j-1)\cdot M/n$ [[Pj=(j-1)·M/n]] of the output clock signal ST compared with the rise timing of the first divided signal SD_1. Assuming that n=8 and M=1024, for example, P2=128, P3=256, . . . , P8=896 respectively. In other words, in the present embodiment as is understood from the above description, any of the given divided signal and the divided signals each having the number adjacent thereto is shifted M/n (e.g., 1025/8=128) in the number of pulses of the output clock signal ST.

Please replace the paragraph bridging pages 14 and 15 the following amended paragraph:

A description has already been made of the case in which the first through n-th divided signals SD1 through SDn of the first through n-th dividers 5_1 ~~51~~ through 5_n ~~5n~~ have been brought to the following relation, i.e., each of the j-th divided signals SBj (where j: an integer of 2 to n) rises with being delayed the number of the pulses $P_j=(j-1)\cdot M/n$ [[Pj=(j-1)·M/n]] of the output clock signal ST compared with the rise timing of the first divided signal SD1. In order to hold the dividers 5_1 ~~51~~ through 5_n ~~5n~~ in such a relationship, the clock multiplying PLL circuit 1 according to the present embodiment is

provided with a divider initial reset circuit 80. The present divider initial reset circuit 80 and its reset method will be described with reference to FIG. 7.

Please replace the first full paragraph of page 17 with the following amended paragraph:

By sequentially resetting the second through n-th dividers 5_2 ~~52~~ through 5_n ~~5n~~ in order, the j-th dividers 5j (corresponding to the second through n-th dividers 5_2 ~~52~~ through 5_n ~~5n~~) can be set in such a manner that the j-th divided signals SBj (where j: an integer of 2 to n) rise with being delayed the number of pulses $P_j=(j-1)\cdot M/n$ [[$P_j=(j-1)\cdot M/n$]] of the output clock signal ST compared with the rising edge of the first divided signal SD1 as described above. Assuming that n=8 and M=1024, for example, P2=128, P3=256, . . . , P8=896 respectively. Since shifts in divided outputs of the dividers 5_1 ~~51~~ through 5_n ~~5n~~ remain unchanged unless the dividers 5_1 ~~51~~ through 5_n ~~5n~~ are reset, the division timings of the dividers 5_1 ~~51~~ through 5_n ~~5n~~ are set in this way, whereby PLL control can be suitably performed subsequently to their settings.